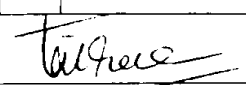


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	AL						<input type="checkbox"/> <input type="checkbox"/>
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	AN						<input type="checkbox"/> <input type="checkbox"/>
	AO						<input type="checkbox"/> <input type="checkbox"/>
	AP						<input type="checkbox"/> <input type="checkbox"/>
<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, etc.)</i>							
TT	AR	Kume et al, "Flash Memory Technology", Ouyou Butsuri, Vol. 65, p. 1114, 1996.					
TT	AS	J.D.Bude et al, "EEPROM/Flash Sub 3.0V Drain-Source Bias Hot Carrier Writing", IEEE International Electron Device Meeting 1995, p. 989-991.					
TT	AT	Ogura et al, "Low Voltage, Low Current, High Speed Program Step Split Gate Cell with Ballistic Direct Injection for EEPROM/Flash", IEEE International Electron Device Meeting, 1998, pp. 987-990.					
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	DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
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	AM					<input type="checkbox"/>	<input type="checkbox"/>
	AN					<input type="checkbox"/>	<input type="checkbox"/>
	AO					<input type="checkbox"/>	<input type="checkbox"/>
	AP					<input type="checkbox"/>	<input type="checkbox"/>

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

TT	AR	T. Jung et al, "A.3.3V 128Mb Multi-Level NAND Flash Memory for Mass Storage Application", IEEE International Solid-State Circuit Conference 1996, pp. 32-33, 1996.
TT	AS	M. Lorenzini et al, "A Dual Gate Flash EEPROM Cell with Two-Bit Storage Capacity", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, Vol. 20, No. 2, p. 182, 1997.
TT	AT	

EXAMINER

DATE CONSIDERED

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